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## APPLICANTS

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## \*\* CONTINUING DATA \*\*\*\*\*

*M31*   *NONE*

## \*\* FOREIGN APPLICATIONS \*\*\*\*\*

JAPAN 2002-251843 08/29/2002  
*my*

## IF REQUIRED, FOREIGN FILING LICENSE GRANTED

\*\* 11/25/2003

Foreign Priority claimed	<input checked="" type="checkbox"/> yes <input type="checkbox"/> no	STATE OR	SHEETS	TOTAL	INDEPENDENT
35 USC 119 (a-d) conditions met	<input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance	COUNTRY	DRAWING	CLAIMS	CLAIMS
Verified and Acknowledged <i>S Hingleton</i> Examiner's Signature	<i>my</i> Initials	JAPAN	8	30	4

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## TITLE

Test method and apparatus for verifying fabrication of transistors in an integrated circuit

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